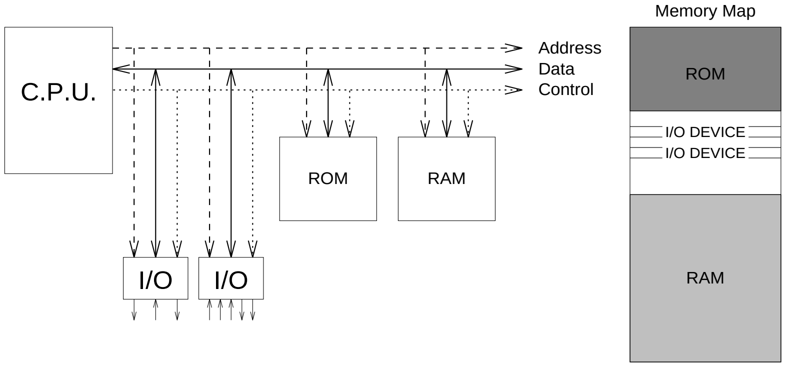
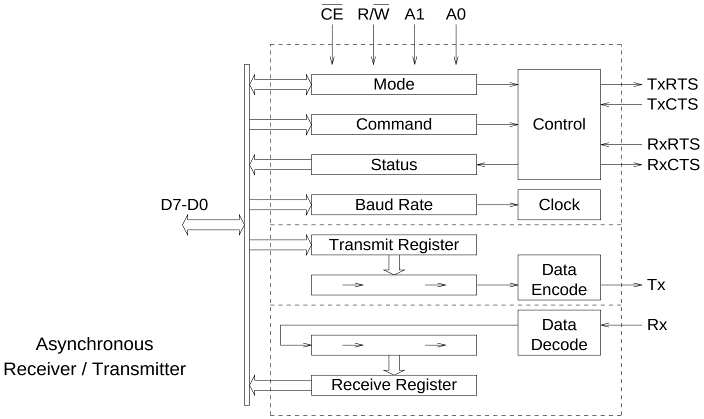
I/O Devices

Memory Mapping

Although some processors have dedicated I/O busses, most share address and data busses with memory.



I/O Devices



I/O Devices

The registers of the asynchronous receiver/transmitter chip[1] are located at the following addresses.

A1,A0	Read	Write
00	Mode	Mode Select
01	Status	Baud Rate Select
10	NOT USED	Command
11	Receive Register	Transmit Register

Register access modes

- read/write
- read only
- write only
- no direct access at all

[1]This chip is loosely based on the SCN2681 DUART as used on ECS SPARCboards.

I/O Devices

Although memory mapped, these registers do not act merely as memory locations used to transfer data. The action of accessing a register provides information to the device.

- Write to *Transmit register* triggers the output of data even if the data in the register is not changed.
- Read from *Receive register* indicates that the data is no longer required so that it may be overwritten.
- Data in the *Command register* is only consulted during a write, its effect is immediate – e.g. reset transmit machine.