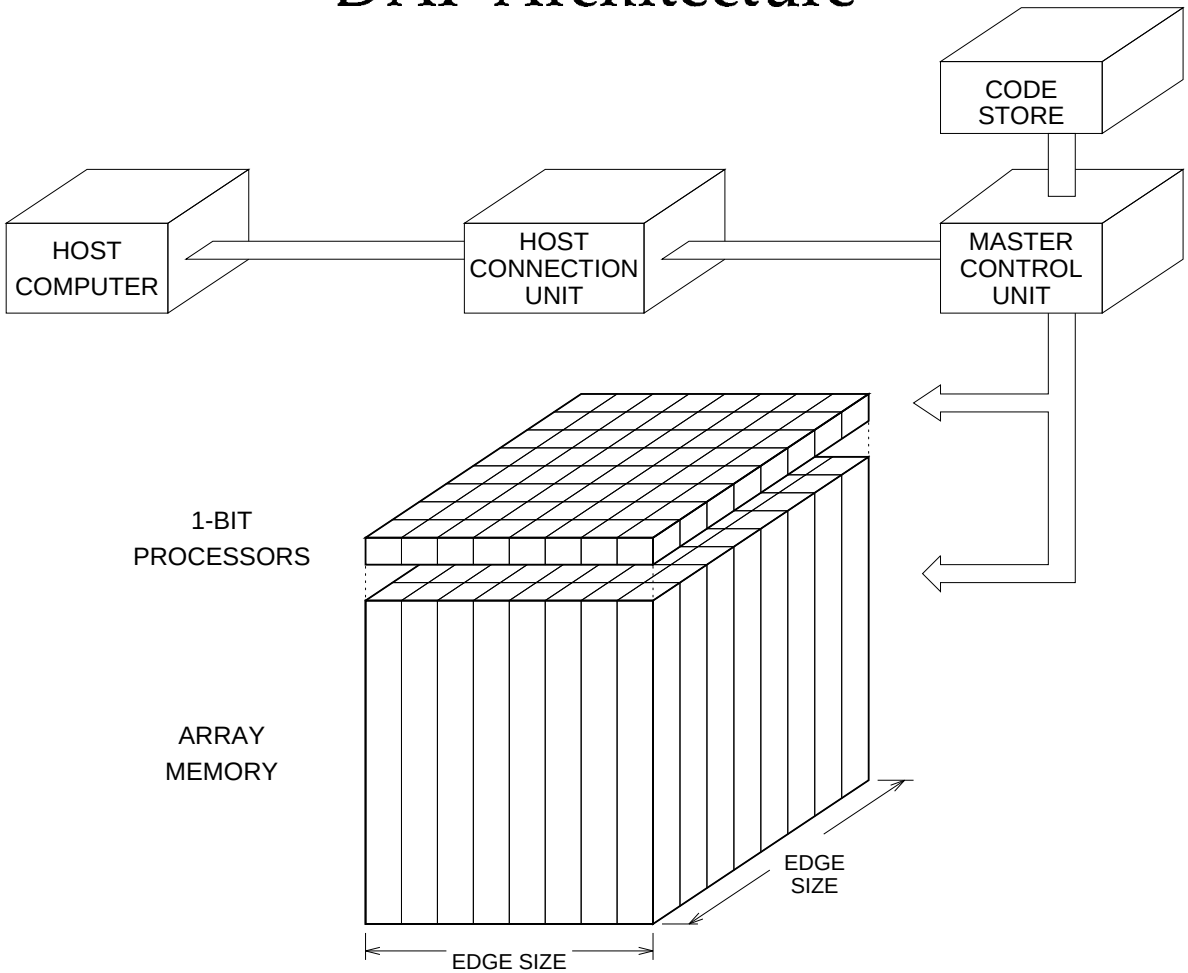
Distributed Array of Processors

- Originally developed by ICL.
- Now built by Active Memory Technology (AMT)
  - Start-up company with ex-ICL employees.
  - Split 50% USA (hardware) and 50% UK (software).
- Massively Parallel SIMD computer.
  - DAP 500 has 1024 PEs
  - DAP 600 has 4096 PEs
- Sun or VAX host.
- Specializes in vision processing and finite element problems.

DAP Architecture



DAP

- Host Computer
  - Provides user interface via keyboard and screen
  - Provides low speed disc I/O for program & data storage.
  - Runs Compilers and Assemblers.
  - Frequently runs sequential parts of code.
- Master Control Unit
  - 32 bit processor
  - Instruction Processing Unit.
  - Controls PEs
  - Controls Memory
  - Makes all global decisions.
  - Special Hardware for DO loops and Address generation.

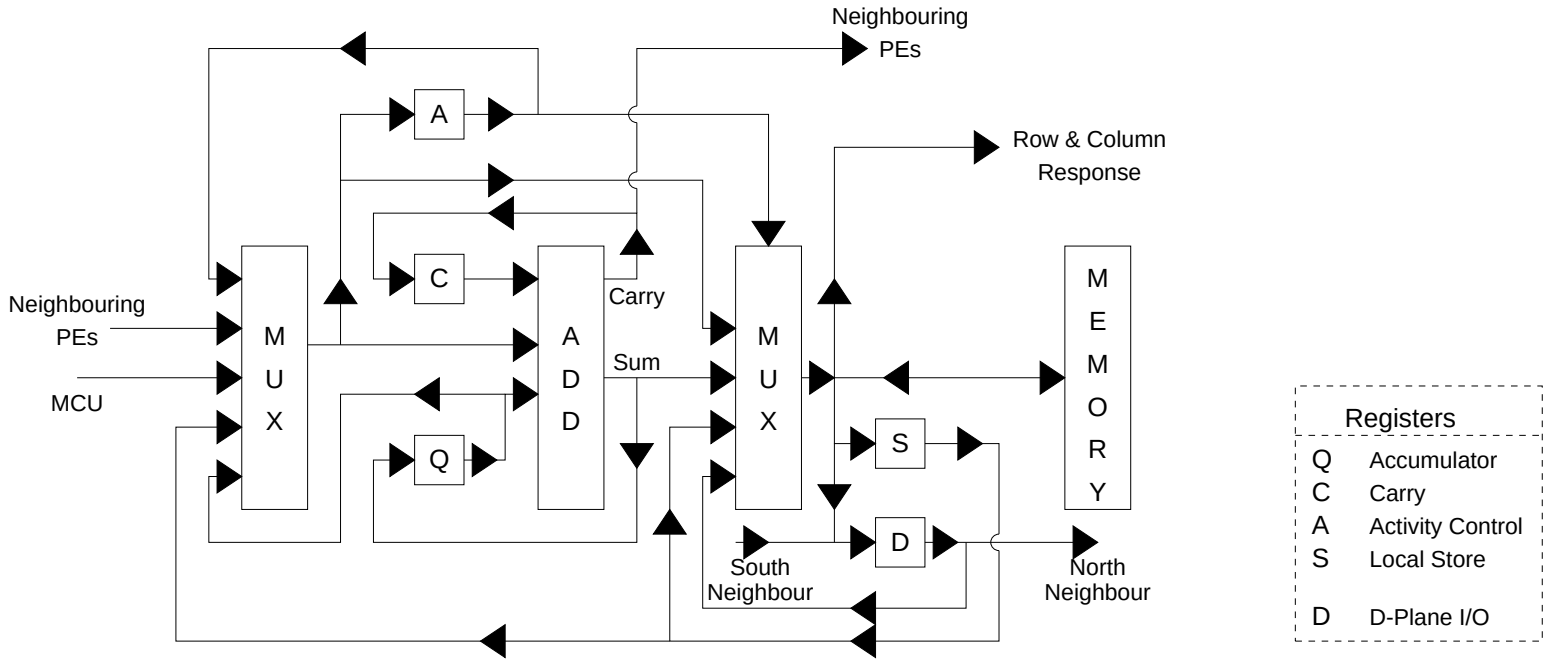
DAP

- Processing Elements & Memory
  - Single bit PEs arranged as a 32x32 or 64x64 grid.
  - 64 PEs per 176 pin chip.
  - Each PE has a 1 bit wide connection to memory.
  - Memory is standard static memory, 32 or 64 kbits per PE.
  - MPU addresses memory.
    Hence a complete plane of memory is accessed at a time.

- Redundancy for error detection
  - Memory planes have parity checks.
  - There are in fact 2048 PEs in a DAP 500
    Each PE is checked by a shadow PE on another chip.

DAP

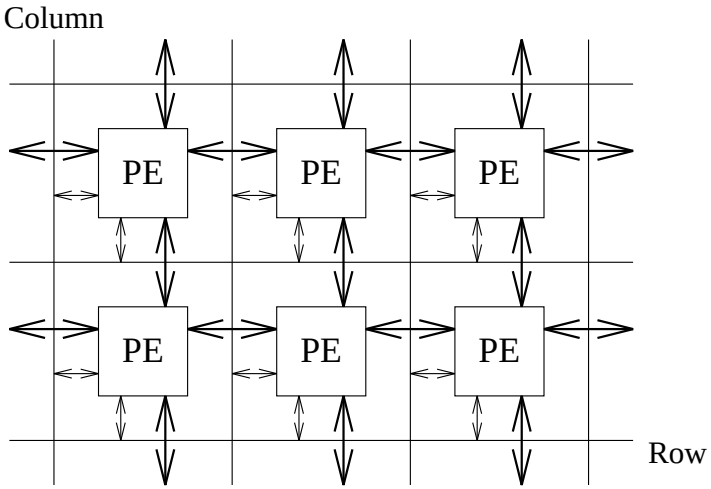
- Processing Element Architecture



– Simple PE
– 1 bit registers & data paths.
– Activity control prevents update of memory from certain PEs.

DAP

- PE connectivity

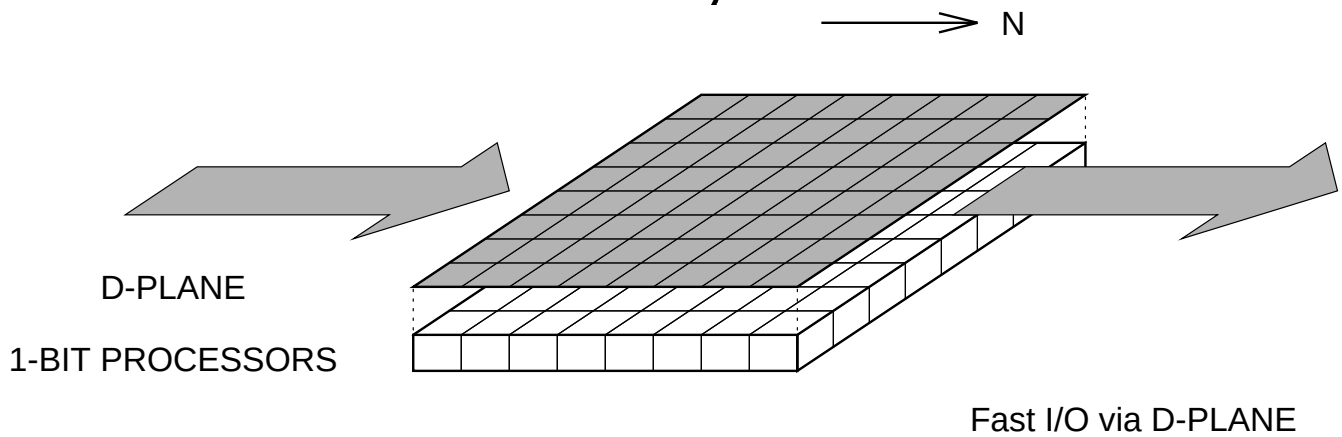


  – N S E & W Nearest neighbour connections:
    - - Allows Q-Plane to be shifted in any direction.
  – Row and Column Highways:
    - - Broadcast from Edge Register.
    - - Wired AND of PE responses to Edge Register.
    - - Select individual row or column for output to Edge Register.

Using Single Bit PEs

- Boolean calculations
  - Very Efficient - Very Powerful.
- Numeric calculations
  - Numbers are normally mapped 'vertically' within the memory of a single PE.
  - The architecture permits 'horizontal' mapping of short vectors for increased efficiency.
- Variable Precision Arithmetic
  - Calculation with reduced precision is carried out at greater speed.
  - Greater efficiency than fixed width processors.

Fast I/O



- High Performance Processing often requires High Bandwidth I/O
- D-Plane is controlled by I/O couplers
  - I/O couplers compete for control of D-Plane and Fast I/O bus.
  - Chosen I/O coupler steals memory cycles for loading and storing from D-Plane.
  - Chosen I/O coupler shifts data *out of* and/or *into* the D-Plane.
  - Shifting can be concurrent with normal processing.

Video I/O

For low speed video I/O it is possible to use the video capabilities of the host. For higher bandwidth applications there are two video I/O couplers available for the DAP.

- Video Display

  1024x1024 pixel 8 bit display mapped onto DAP array memory.

  – Computer Graphics
  – Data Visualization

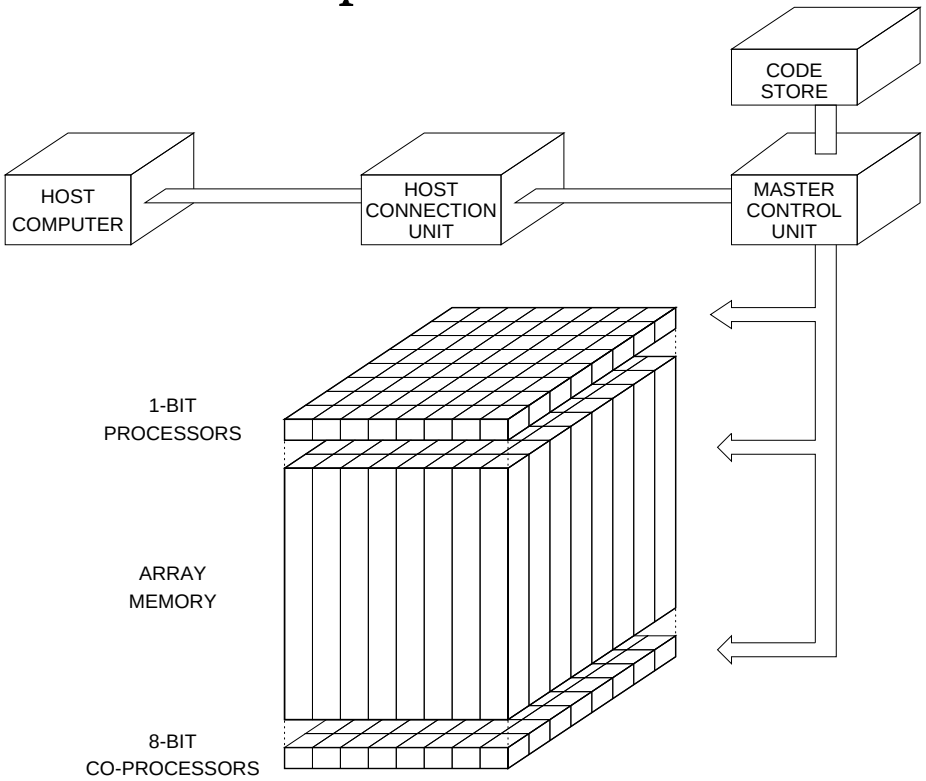
- Frame Grabber

  Allows colour pictures (moving and static) to be loaded into array memory.

  – Computer vision applications - feature extraction etc.
  – Real Time image processing - using Video display.

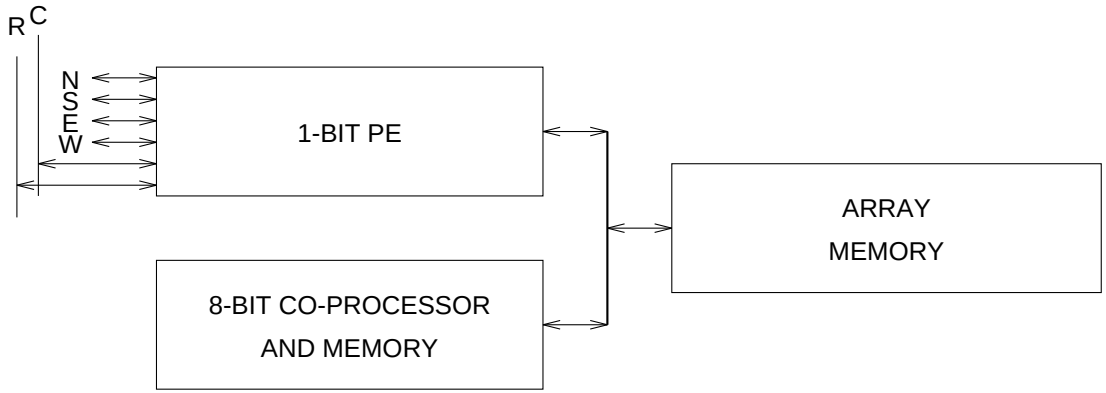
CP8 Co-Processor

For improved floating point performance each PE may optionally be provided with an 8-bit co-processor.



CP8 Co-Processor

- Data Paths
  - 1-bit PE communicates with memory, other PEs and the MCU but not with the co-processor.
  - 8-bit co-processor communicates only with memory via a 1-bit wide data-path.



  - The co-processor has a number of internal 8-bit registers for the storage of operands.

CP8 Co-Processor

- 1-Bit PE performs inter-PE communication and boolean manipulation.
- 1-Bit PE communicates with co-processor via shared memory.
- 8-bit co-processor is used for multi-bit arithmetic.
- Operation of co-processor.
  - Copy operand data from array memory to co-processor memory (1-bit at a time).
  - Perform operation in co-processor memory.
  - Copy results back to array memory.

N.B. A larger co-processor would cause an imbalance between processor power and memory bandwidth.

Software

- Host Program
  - Provides a screen & keyboard interface, does disc I/O and scalar processing.
  - Fortran 77 or C
  - Communicates with the DAP via a *Common Data Block*
  - Makes calls to DAP routines.
- DAP Program
  - Performs array processing and high speed I/O via D-Plane.
  - Fortran Plus *Data Parallel* language.
  - Unconstrained Fortran Plus arrived with DAP 600
  - Fortran 90 - yet to come.