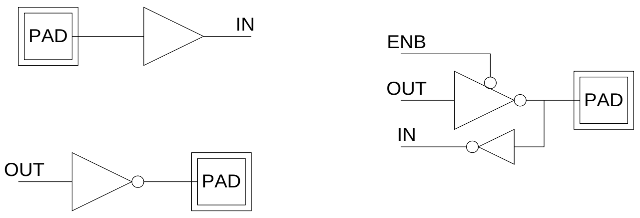
Input / Output

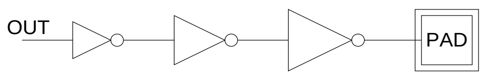
- I/O Pads



  – A brief look at a selection of simple digital CMOS I/O pads

Output Pads

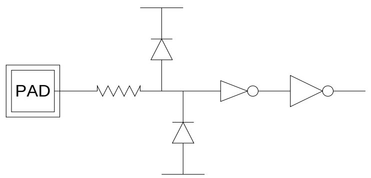
- Output pad driver



  – ratioed inverters are used to provide appropriate drive capability
  – final drive transistors are carefully designed to avoid latch-up
  – pad rings are frequently powered separately (dirty power) to confine switching noise

Input Pads

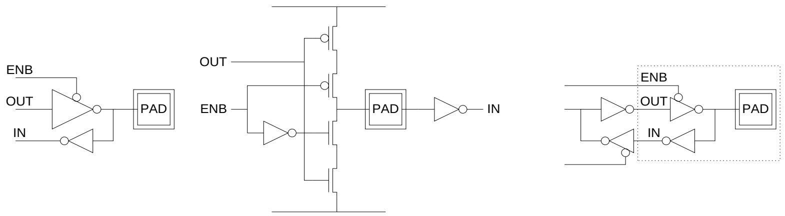
- Input protection



  – must protect floating transistor gates from permanent damage via electrostatic discharge

Bidirectional Pads

- Simple bidirectional pad

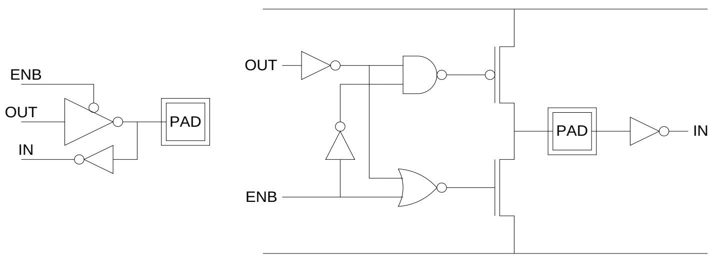


  – bidirectional pad is a tristate inverter output driver combined with an input pad[1]
  – If `IN` and `OUT` are connected internally, we need buffering and an input enable control signal

[1] note input protection is not shown here

Bidirectional Pads

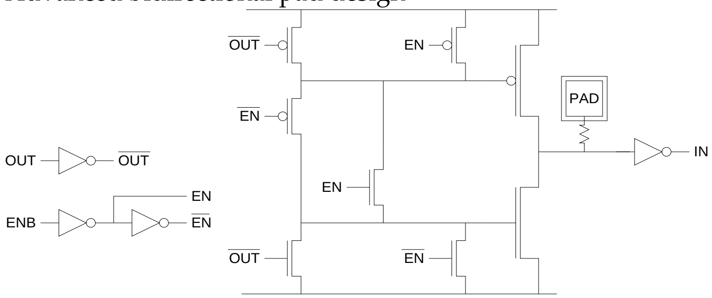
- Bidirectional pad with increased drive capability



  - redesign to avoid series output transistors

Bidirectional Pads

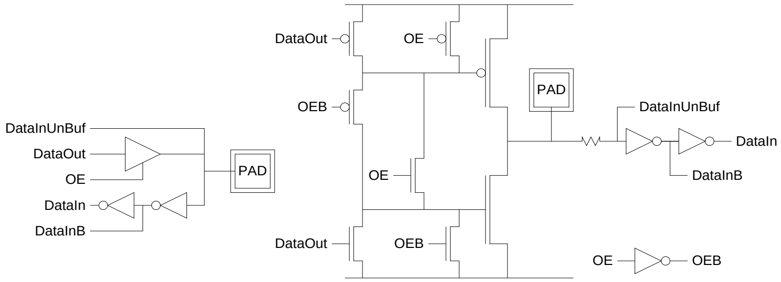
- Advanced bidirectional pad design



  - logic gates are merged
  - output transistors act as diodes when not enabled
  - low value diffusion resistor completes input protection circuit

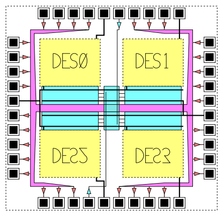
Bidirectional Pads

- MOSIS Bidirectional Pads

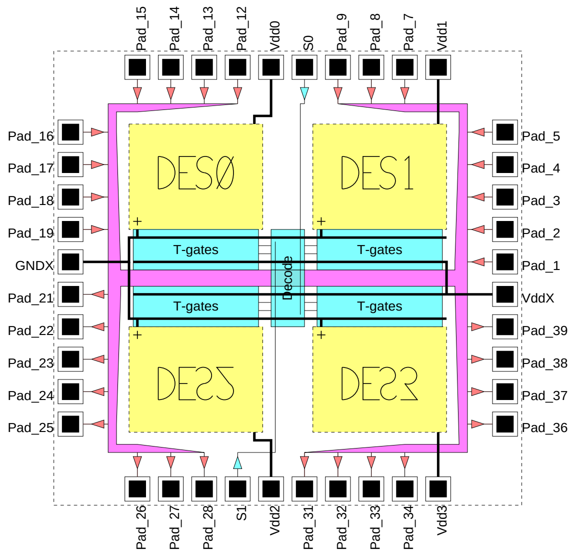


  - less buffering on DataOut from core circuit

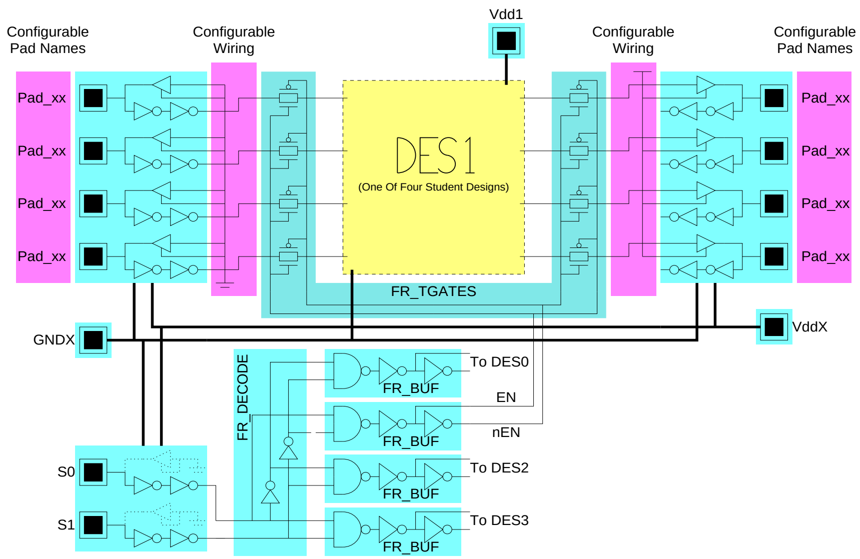
UoC Tiny Chip



- 40 Pad MOSIS AMI 0.5μm TinyChip Frame 1500μm × 1500μm
- 4 Designs ≈430μm × ≈380μm
- 32 User I/O Pins (pre-selected as either input or output)
- Complete isolation of designs not under test


Pad_15
Pad_14
Pad_13
Pad_12
Vdd0
S0
Pad_9
Pad_8
Pad_7
Vdd1
Pad_16
Pad_17
Pad_18
Pad_19
GNDX
Pad_21
Pad_22
Pad_23
Pad_24
Pad_25
Pad_5
Pad_4
Pad_3
Pad_2
Pad_1
VddX
Pad_39
Pad_38
Pad_37
Pad_36
DES0
DES1
DES2
DES3
T-gates
T-gates
T-gates
T-gates
Decode
Pad_26
Pad_27
Pad_28
S1
Vdd2
Pad_31
Pad_32
Pad_33
Pad_34
Vdd3

10009


Configurable Pad Names
Configurable Wiring
Vdd1
Configurable Wiring
Configurable Pad Names
Pad_xx
Pad_xx
Pad_xx
Pad_xx
DES1
(One Of Four Student Designs)
Pad_xx
Pad_xx
Pad_xx
Pad_xx
FR_TGATES
GNDX
VddX
FR_DECODE
To DES0
FR_BUF
EN
nEN
FR_BUF
To DES2
FR_BUF
To DES3
FR_BUF
S0
S1

10010