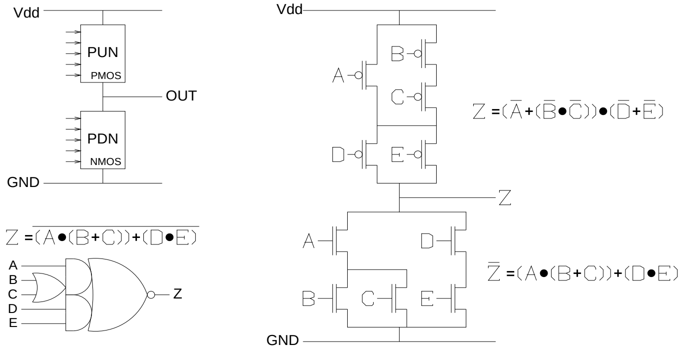
## Static CMOS Complementary Gates

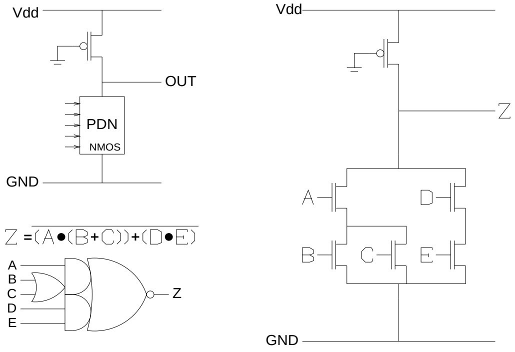



- For any set of inputs there will exist **either** a path to Vdd **or** a path to GND.
- No transistor sizing is necessary for circuit function[1].
  Minimum geometry transistors may be used.

[1] although transistor sizing may improve performance



## Pseudo-NMOS Gates

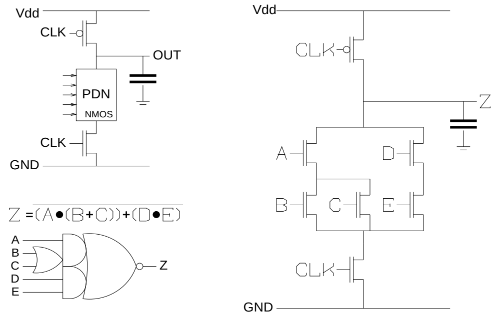



- Compact design with fewer transistors.
- Weak P channel device is always on.[2]

[2] $W_p$:$W_n$ ratio determines gate speed, static power consumption and low output voltage.



## Dynamic CMOS Gates

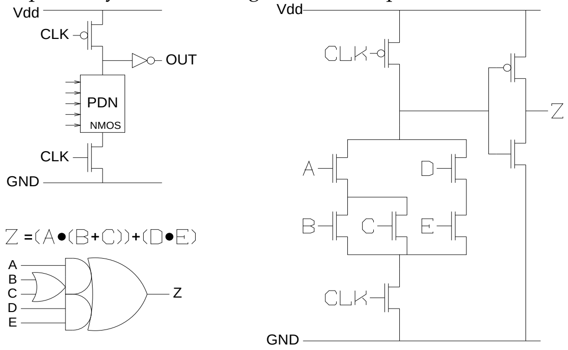



- Precharge Phase (CLK=0) Output is precharged to Vdd.
- Evaluate Phase (CLK=1) Output is conditionally discharged to GND.
  Evaluation is very fast since there is no pull-up.
- Output capacitor is primarily the gate capacitance of subsequent transistors.



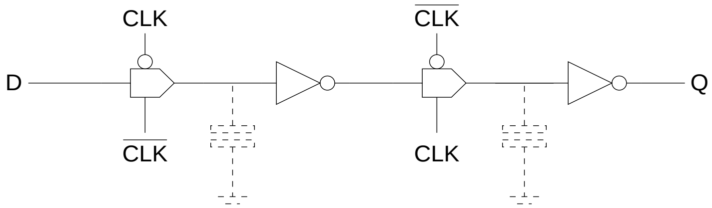
## CMOS Domino Gates

Dynamic gates can not be cascaded with other dynamic gates using the same clock phase since inputs may not fall during the evaluate phase.




- Domino gates can be cascaded.
- Only non-inverting structures are possible.

## Dynamic CMOS D-Type

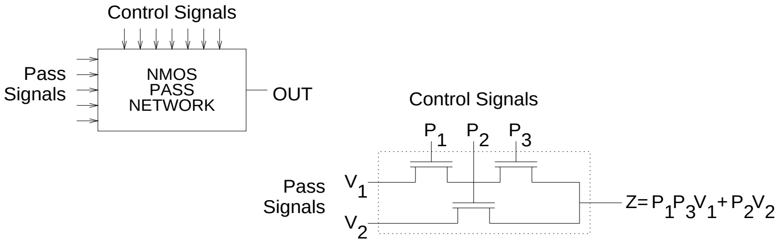



- Very fast Master Slave D-Type
- Minimum clock speed is determined by charge leakage.

*Dynamic D-Types are often used in conjunction with static logic gates. Similarly static D-Types may be used alongside dynamic logic gates.*



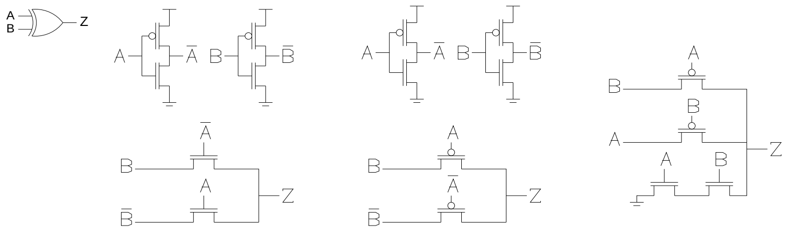
## Pass Transistor Circuits




- Provides very compact circuits.
- Good transmission of logic '0'.
- Poor transmission of logic '1'.
  - slow rise time
  - degradation of logic value



## Pass Transistor Gates



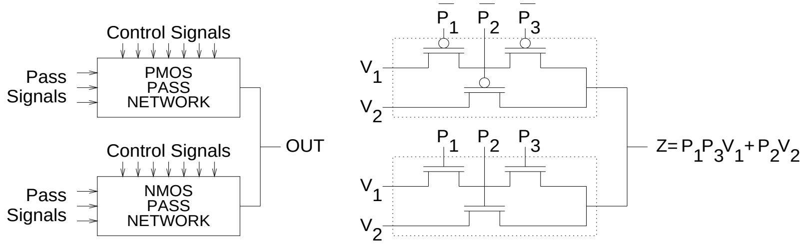

- Pass transistor circuits can also be built with PMOS transistors
  - Good transmission of logic '1'.
  - Poor transmission of logic '0'.

  or a mixture of NMOS & PMOS.

*These compact gates may come at the expense of very poor performance, particularly for transistors with larger values of threshold voltage.*



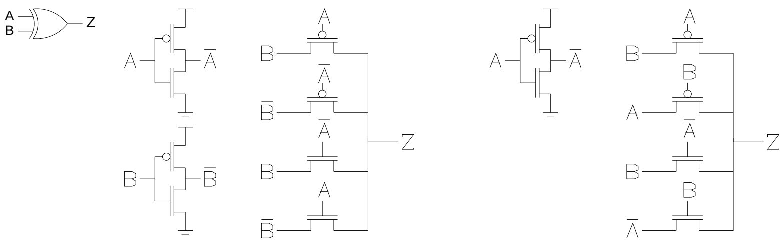
## Complementary Pass Transistor Circuits



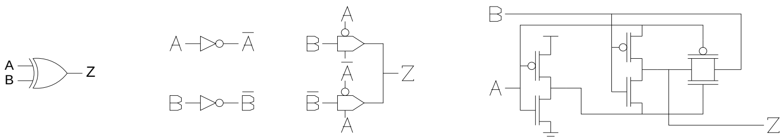

- For good pull-up and pull-down performance we need complementary networks.

  Although this may simply replace pass transistors with transmission gates, optimizations are possible where:
  - PMOS network passes all '1's — but not necessarily all '0's
  - NMOS network passes all '0's — but not necessarily all '1's

# Complementary Pass Transistor Gates

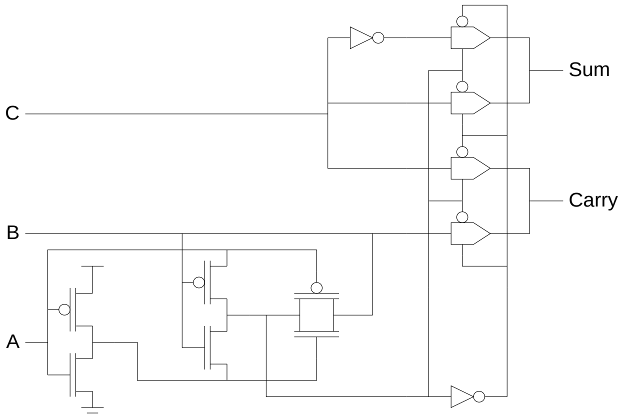



The first design employs a transmission gate multiplexor while the second is the standard 6 transistor XOR:






# Complementary Pass Transistor Gates




An 18 transistor full adder may be constructed making use of both XOR designs.