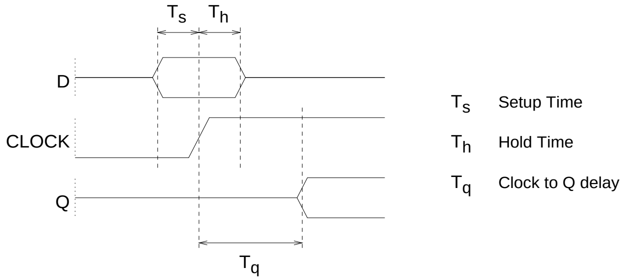
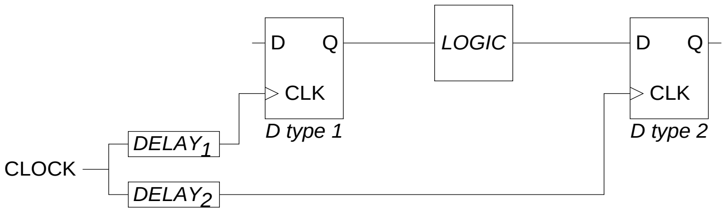
D type Timing

- Timing



  - Valid data should be present on D input for at least T_s before the active clock edge and at least T_h after the clock edge.
  - The minimum D type cycle time will be limited by the sum $T_s + T_q$.

D type Timing



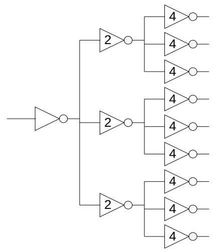
- Hold violation caused by clock skew
  - *D-type 1* clocks first, D input of *D-type 2* changes too early

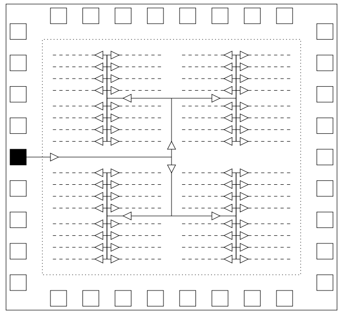
    May occur if difference in clock delays (clock skew) is greater than the delay due to logic and wiring between Q_1 and D_2.[1]

[1] A certain amount of leeway is possible determined by the D-Type characteristics, T_q - T_h

Clock Distribution

- Skew reduction

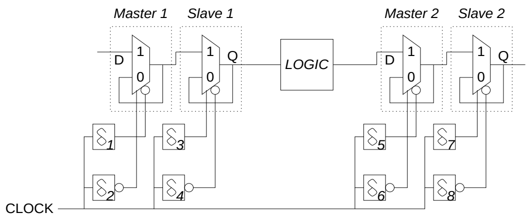




  - clock distribution tree
  - match all clock paths
  - greater clock buffer drive strength will reduce the skew due to imbalance in buffer loadings

D type Timing

- Race hazards with Master Slave D-Types



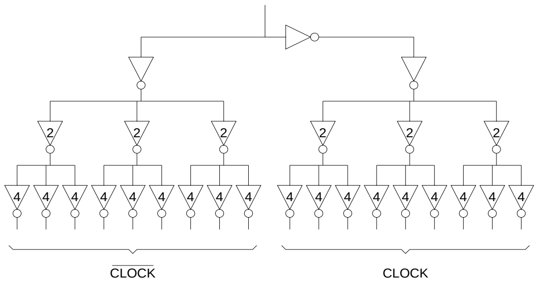
  - Rising CLOCK edge

    Delayed latching of *master 2* may leave *slave 1* and *master 2* transparent simultaneously. Data is then transferred in error from *master 1* to *slave 2*.
  - Falling CLOCK edge

    Delayed latching of *slave 1* may leave *master 1* and *slave 1* transparent simultaneously. Q_1 will then change in error mid-cycle.

Clock Distribution

- Skew reduction for $clock$ and $\overline{clock}$[2]

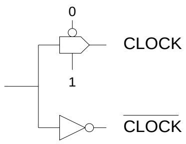


  - minimum load on inverter creating skew
  - note $clock$ and $\overline{clock}$ signals should be routed together to balance routing delays.

[2] we could alternatively generate $\overline{clock}$ locally within each master slave D Type.

Clock Distribution

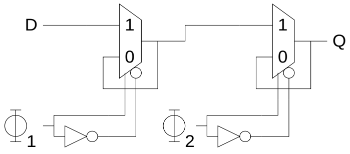
- Skew elimination

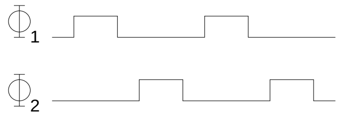


  - eliminates skew caused by single inverter
  - size transistors to equalize delay
  - ensure that load and drive strengths are taken into account

Clock Distribution

- Non-overlapping clocks

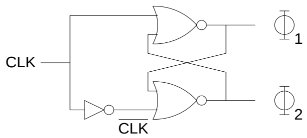


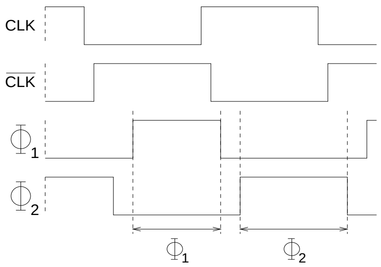


  - guarantees only one latch transparent at any one time

Clock Distribution

- Non-overlapping clocks

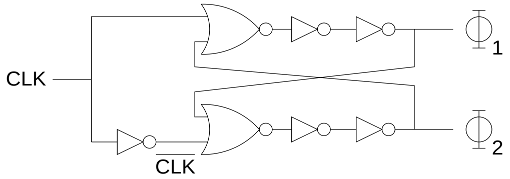




  - clock generation circuit
  - this circuit provides clocks which are non-overlapping active high, suitable for use with latches which are transparent with a high clock input.

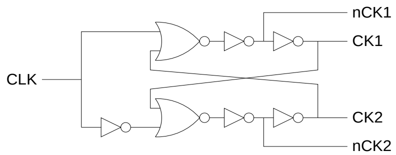
D type Timing

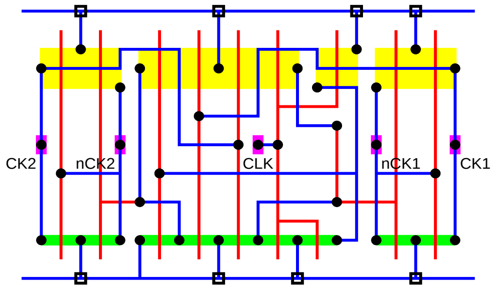
- Non-overlapping clocks



  - inverters provide additional delay to separate phases, may also be the clock buffers
  - time between master transparent and slave transparent is wasted
  - although we can now cope with large skew it is better to avoid it

Two Phase Clock Generator (CLKGEN)





Non-Inverting Buffer (BUF)