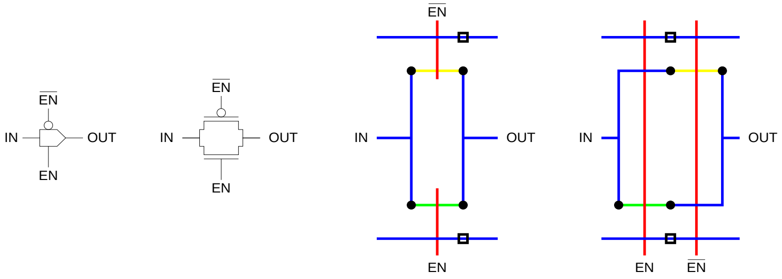
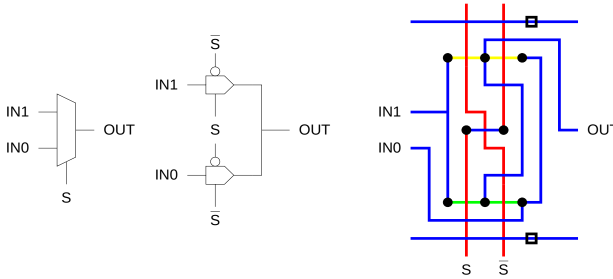
Transmission Gate



Note that transmission gate circuits are not fully complementary[1] hence they do not immediately lend themselves to a *line of diffusion* implementation.

[1] since there are sets of inputs for which the output is neither pulled low nor high

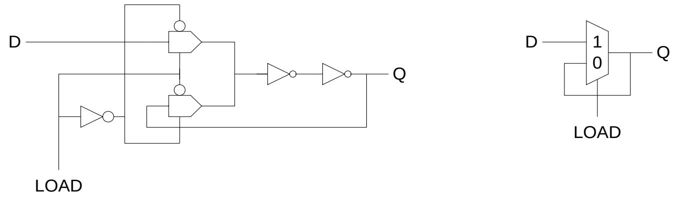
Transmission Gate Multiplexor



- very few transistors 4 (+2 for inverter)
- difficult layout may offset this advantage
  - prime candidate for 2 level metal

Storage elements

- CMOS transmission gate latch

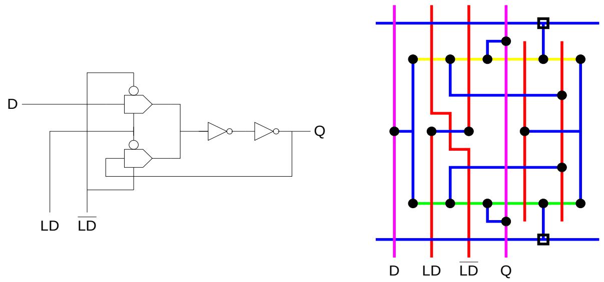


A simple transparent latch can be build around a transmission gate multiplexor

- transparent when load is high
- latched when load is low
- two inverters are required since the transmission gate cannot drive itself

Storage elements

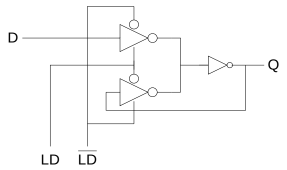
- Transmission gate latch layout

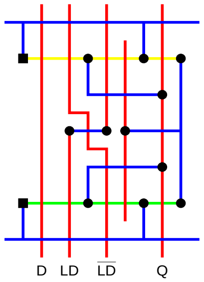


- a compact layout is possible using 2 layer metal

Storage elements

- A simpler layout may be achieved using tristate inverters.

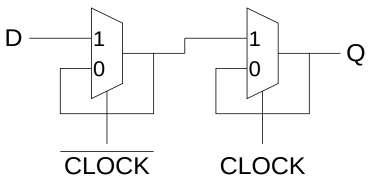




  – this design requires two additional transistors but may well be more compact.

Storage elements

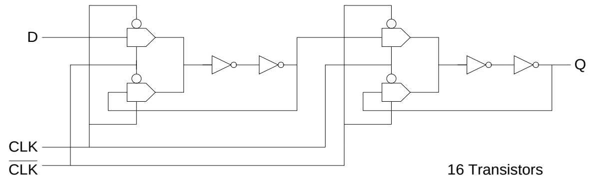
- For use in simple synchronous circuits we use a pair of latches in a master slave configuration.



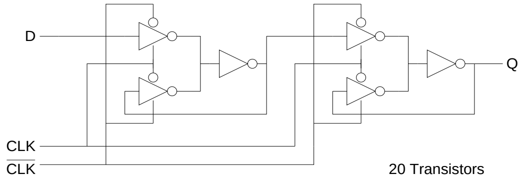
  – this avoids the race condition in which a transparent latch drives a second transparent latch operating on the same clock phase.
  – the circuit behaves as a rising edge triggered D type flip-flop.

Storage elements

- Transmission gate implementation

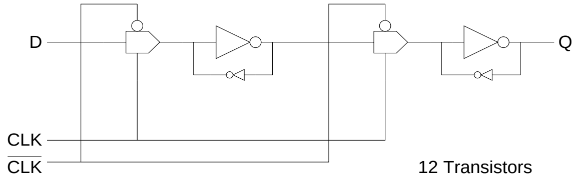


- Tristate inverter implementation

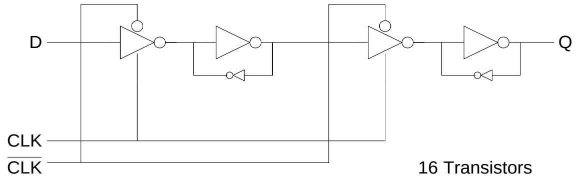


Storage elements

- Transmission gate implementation using keepers

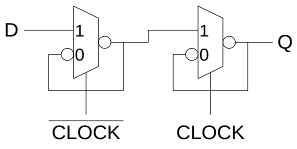


- Tristate inverter implementation using keepers

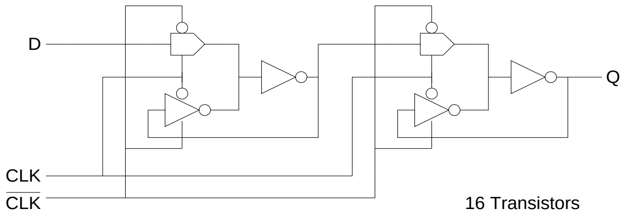


Storage elements

- Alternative configuration

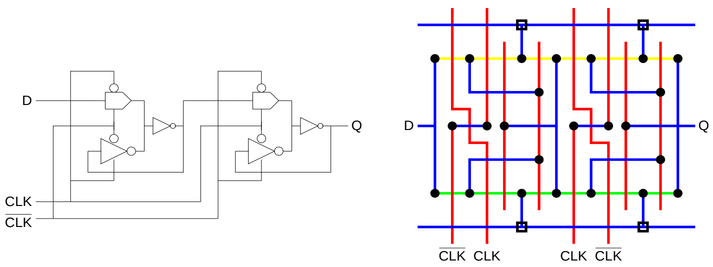


  – Implementation



Storage elements

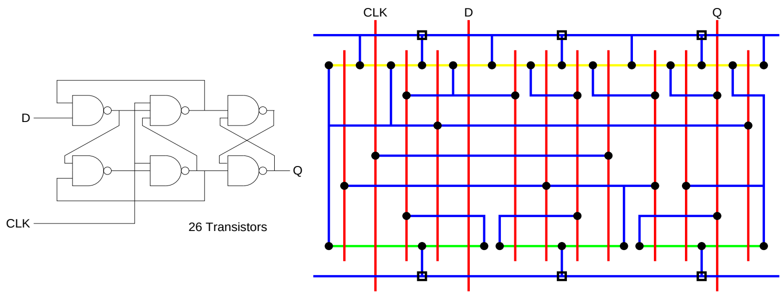
- Layout of master slave D type.



  – very compact using alternative configuration.

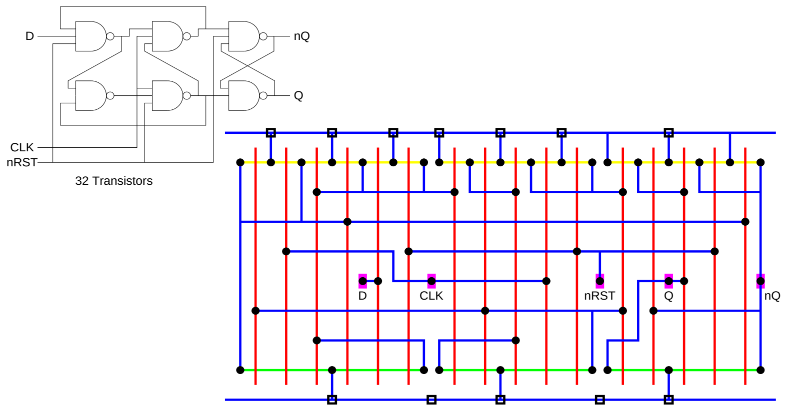
Storage elements

- For the same functionality we could use an edge triggered D type:

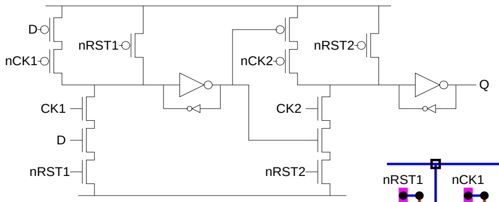


  – a few more transistors
  – more complex wiring
  – simpler clock distribution

Edge Triggered D-Type with Reset (DFFR)



Master Slave D-Type with Reset (MSDR)



20 Transistors