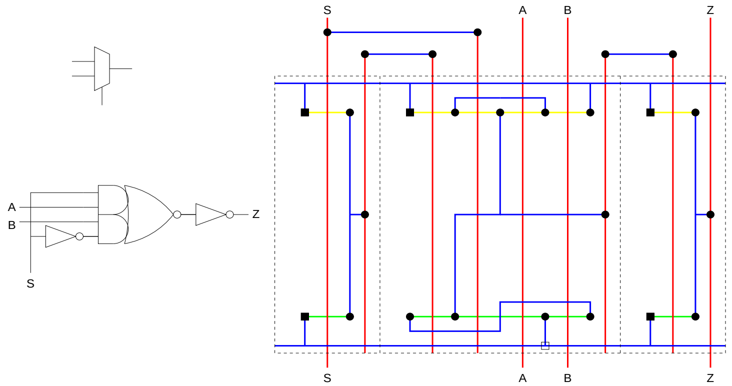
Digital CMOS Design

Multiple gates



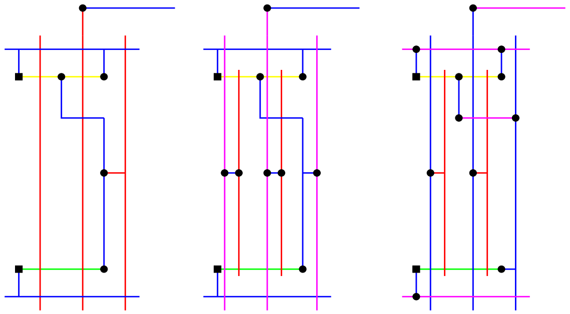
Digital CMOS Design

Multiple gates

- Gates should all be of same height.
  - Power and ground rails will then line up when butted.
- All gate inputs and outputs are available at top and bottom.
  - All routing is external to cells.
  - Preserves the benefits of hierarchy.
- Interconnect is via *two conductor routing*.
  - In this case Polysilicon vertically and Metal horizontally.

Digital CMOS Design

Two-layer Metal



Most modern VLSI processes support two or more metal layers. The norm is to use only metal for inter-cell routing. Either Metal1 horizontally (and for power rails) and Metal2 vertically (and for cell inputs and outputs) or vice versa.

Standard Cell Design

Many ICs are designed using the standard cell method.

- Cell Library Creation

  A cell library, containing commonly used logic gates, is created for a process. This is often carried out by or on behalf of the foundry.

- ASIC[1] Design

  The ASIC designer must design a circuit using the logic gates available in the library.

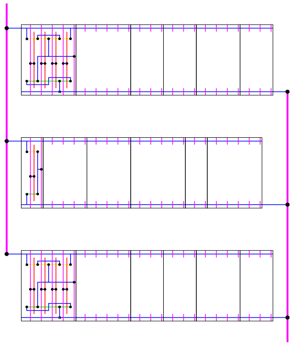
  The ASIC designer usually has no access to the full layout of the standard cells and doesn't create any new cells for the library.

  Layout work performed by the ASIC designer is divided into two stages:

  - Placement
  - Routing

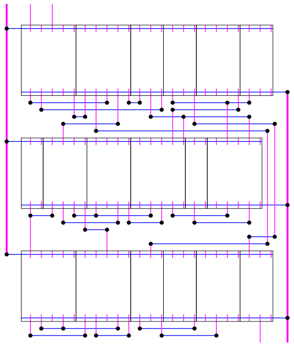
[1] Application Specific Integrated Circuit

Placement



Cells are placed in one or several equal length lines with inter-digitated power and ground rails.

Routing



In the routing channels between the cells we route metal1 horizontally and metal2 vertically.

Two conductor routing

- This logical approach means that we should never have to worry about signals crossing.

  This makes life considerably easier for a computer (or even a human) to complete the routing.
- We must only ensure that two signals will not meet in the same horizontal or vertical channel.
- Computer algorithms can be used to ensure placement of cells such that wires are short.[2]
- Further computer algorithms can be used to optimize the routing itself.

[2] In VLSI circuits we often find that inter-cell wiring occupies more area than the cells themselves.

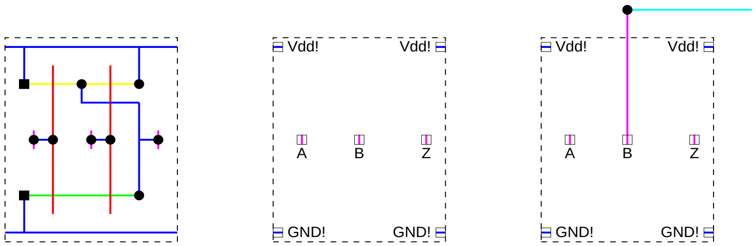
More Metal Layers

With three or more metal layers it is possible to take a different approach.
The simplest example uses three metal layers.

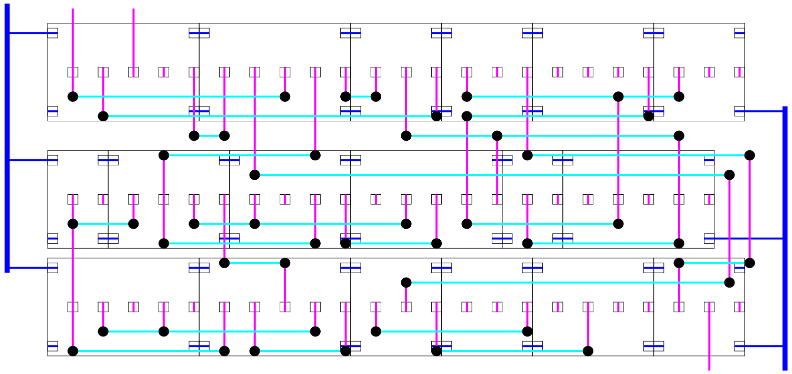
- Standard Cells

  Use only metal1 except for I/O which is in metal2
- Two Conductor Routing

  Uses metal2 and metal3



More Metal Layers



With this approach we can route safely over the cell to the specified pins leading to much smaller gaps between cell rows.