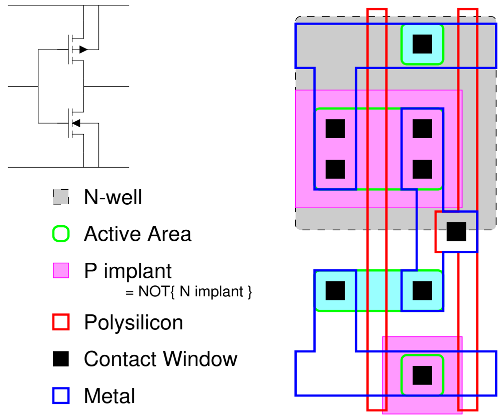
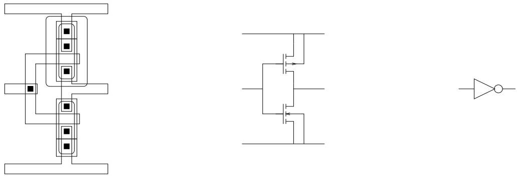
Mask Level Design

0.5 μm CMOS inverter



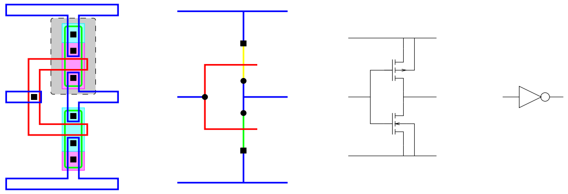
Abstraction

Levels of Abstraction



- Mask Level Design
  - Laborious Technology/Process dependent.
  - Design rules may change during a design!
- Transistor Level Design
  - Process independent, Technology dependent.
- Gate Level Design
  - Process/Technology independent.

Abstraction - Stick Diagrams



Stick diagrams give us many of the benefits of abstraction:

- Much easier/faster than full mask specification.
- Process independent (valid for any CMOS process).
- Easy to change.

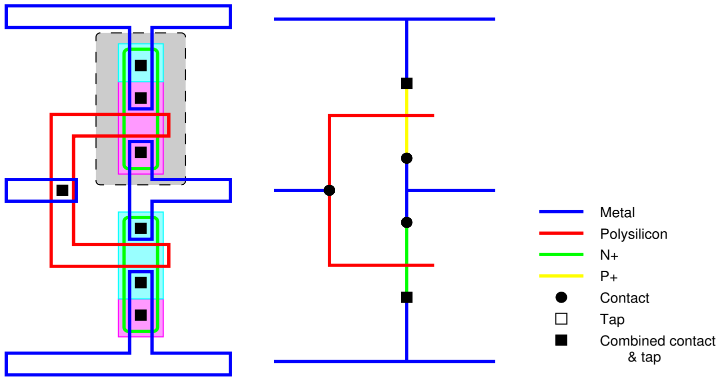
while avoiding some of the problems:

- Optimized layout may be generated much more easily from a stick diagram than from transistor or gate level designs.[1]

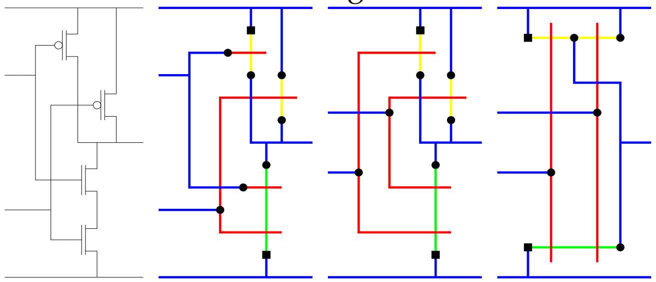
[1]note that all IC designs must end at the mask level.

Digital CMOS Design

Stick Diagrams



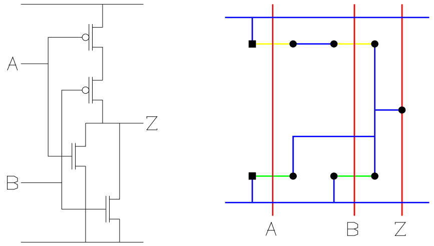
Stick Diagrams



- *Explore your Design Space.*
  - Implications of crossovers.
  - Number of contacts.
  - Arrangement of devices and connections.

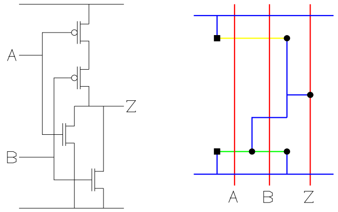
A logical approach to gate layout.

- *All complementary gates may be designed using a single row of n-transistors above or below a single row of p-transistors, aligned at common gate connections.*



Euler Path

- For the majority of these gates we can find an arrangement of transistors such that we can butt adjoining transistors.
  - Careful selection of transistor ordering.
  - Careful orientation of transistor source and drain.
- Referred to as *line of diffusion*.



Finding an Euler Path

Computer Algorithms

- It is relatively easy for a computer to consider all possible arrangements of transistors in search of a suitable Euler path.

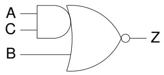
  This is not so easy for the human designer.

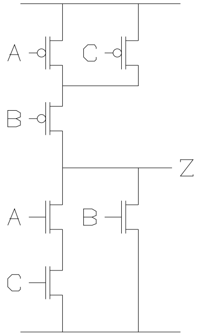
One Human Algorithm

- Find a path which passes through all n-transistors exactly once.
- Express the path in terms of the gate connections.
- Is it possible to follow a similarly labelled path through the p-transistors?
  - Yes – you've succeeded.
  - No – try again (you may like to try a p path first this time).

Finding an Euler Path

$Z = \overline{(A \bullet C) + B}$



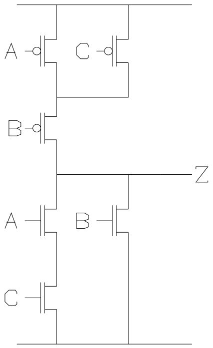


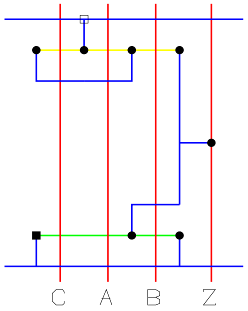
- A−C−B
- B−A−C
- B−C−A
- C−A−B ⇐

- A−B−C
- A−C−B
- B−A−C
- B−C−A
- C−A−B ⇐
- C−B−A

Here there are four possible Euler paths.

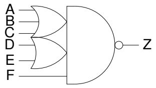
Finding an Euler Path

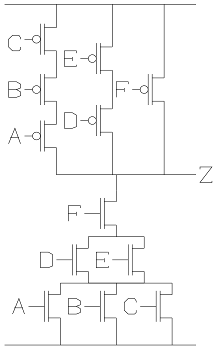




Finding an Euler Path

$Z = \overline{(A+B+C) \bullet (D+E) \bullet F}$

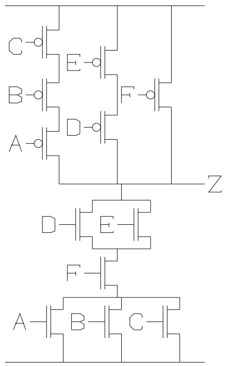


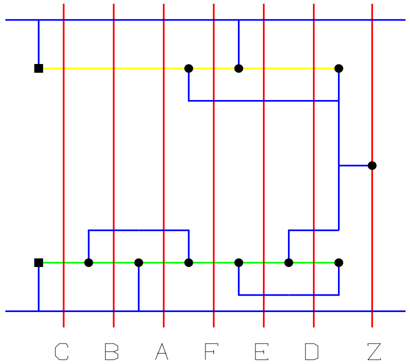


No possible path through n-transistors!

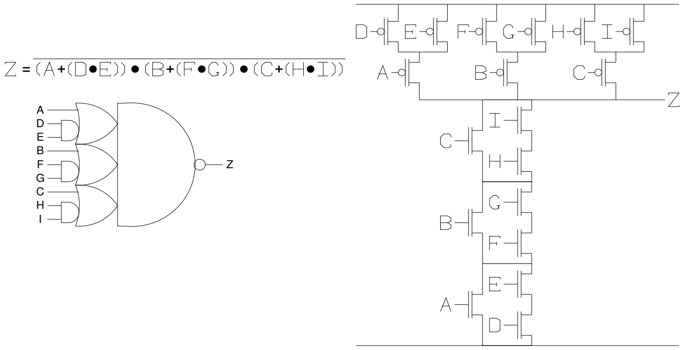
Finding an Euler Path

$Z = \overline{(A+B+C) \bullet (D+E) \bullet F}$





Finding an Euler Path



No possible path through p-transistors.
No re-arrangement will create a solution!