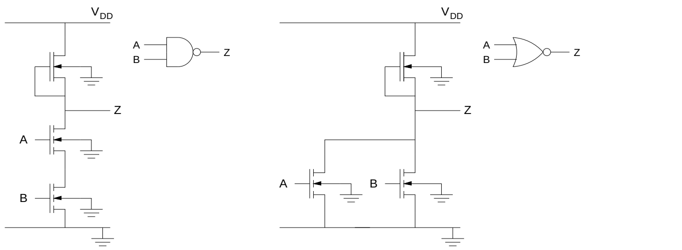
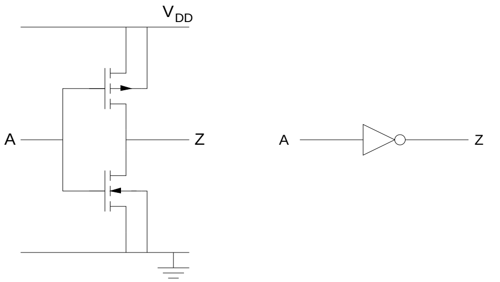
NMOS VLSI technology



- Circuit function determined by series/parallel combination of devices.
- Depletion transistor acts as a *small geometry* non-linear load resistor.

  Resistance increases as the enhancement device turns on, thus reducing power consumption.
- The low output voltage is determined by the size ratio of the devices.

CMOS - *state of the art* VLSI technology



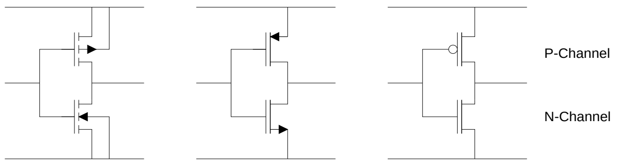
- An active PMOS device complements the NMOS device giving:
  - rail to rail output swing.
  - negligible static power consumption.

Since transistor sizing is not a pre-requisite of CMOS technology[1]. We can use minimum geometry transistors giving a significant saving in area.

[1] Transistor sizing can be used to optimize performance at the expense of area.

Digital CMOS Circuits

Alternative representations for CMOS transistors

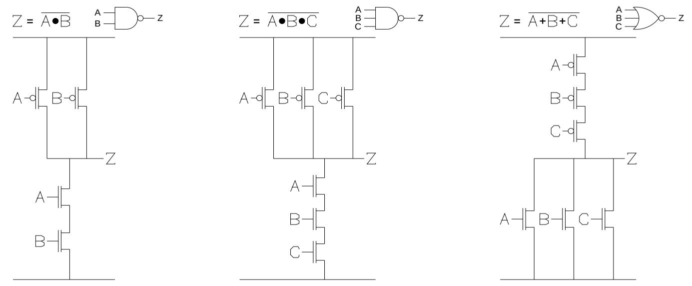


Various shorthands are used for simplifying CMOS circuit diagrams.

- In general substrate connections are not drawn where they connect to Vdd (PMOS) and Gnd (NMOS).
- All CMOS devices are enhancement mode.
- Transistors act as simple digitally controlled switches.

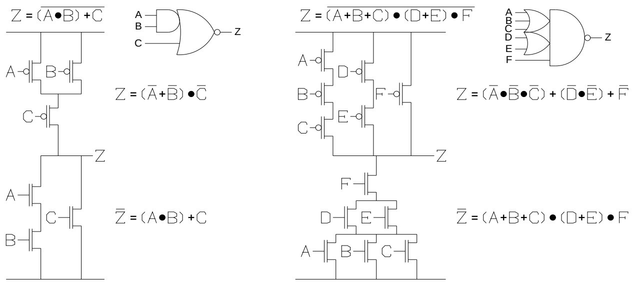
Digital CMOS Circuits

Static CMOS complementary gates



- For any set of inputs there will exist either a path to Vdd or a path to Gnd.

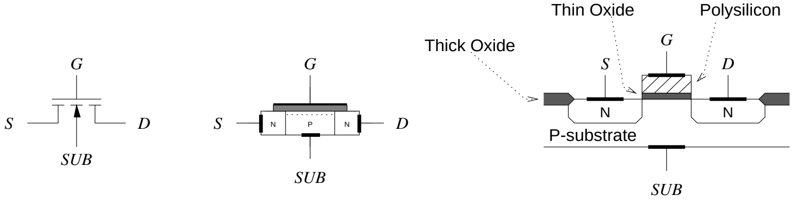
Compound Gates

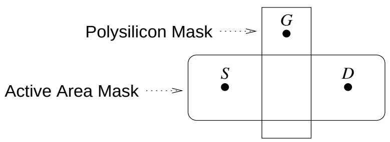


- All compound gates are inverting.
- Realisable functions are arbitrary AND/OR expressions with inverted output.

MOS Transistors

Simple NMOS Transistor



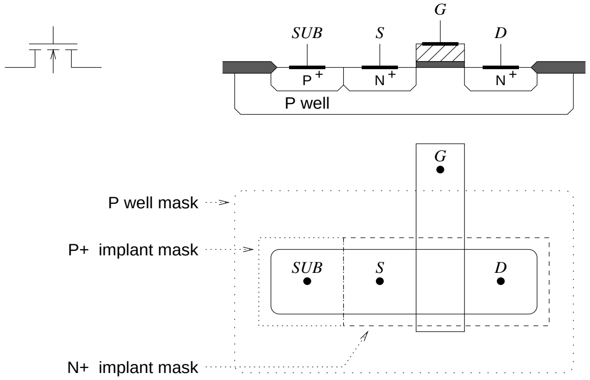


Simple NMOS Transistor

- Active Area mask defines extent of *Thick Oxide*.
- Polysilicon mask also controls extent of *Thin Oxide* (alias *Gate Oxide*).
- N-type implant has no extra mask.
  – It is blocked by thick oxide and by polysilicon.
  – The implant is *Self Aligned*.
- Substrate connection is to bottom of wafer.
  – All substrates to ground.
- Gate connection not above transistor area.
  – Design Rule.

MOS Transistors

NMOS Transistor



Components for Digital IC Design

NMOS Transistor

Where it is not suitable for substrate connections to be shared, a more complex process is used.

- Five masks must be used to define the transistor:
  - P Well
  - Active Area
  - Polysilicon
  - N+ implant
  - P+ implant
- P Well, for isolation.
- Top *substrate* connection.
- P+/N+ implants produce good *ohmic* contacts.

CMOS Process

CMOS Inverter

- The process described here is an *N Well process* since it has only an N Well.

  P Well and Twin Tub processes also exist.
- Note that the P-N junction between chip substrate and N Well will remain reverse biased.

  Thus the transistors remain isolated.
- N implant defines NMOS source/drain and PMOS substrate contact.
- P implant defines PMOS source/drain and NMOS substrate contact.

CMOS Process

CMOS Inverter