Integrated Circuit Engineering 2

Iain McNally

Visiting from **University of Ìì·¢ÓéÀÖÆåÅÆ_Ìì·¢ÓéÀÖAPP-¹Ù**

Room A304 x7267

≈ 13 lectures + 3 labs

≈ 1 Exam Question

Chip Design Assignment

Integrated Circuit Engineering 2

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- Lectures CMOS Design
  - CMOS Gate Design and Compound Gates
  - Cell Design and Euler Paths
  - System Design using Standard Cells
  - Bitslice Design
  - Storage
  - Dynamic Logic
  - High Level Design
  - Design Automation

Integrated Circuit Engineering 2

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- Labs
  - L-Edit / T-Spice
  - S-Edit
  - Space
    Digital Simulation and Accurate Analogue Simulation
- Notes & Resources
  - `http://www.elec.canterbury.ac.nz/support/courses/3rdPro/435/bim`
- Book
  - **Principles of CMOS VLSI Design**
    A systems Perspective
    Neil Weste & Kamran Eshraghian
    Addison-Wesley

Lecture/Lab Schedule

Week 1	Mon 24^{th} Feb	Intro to Assignment	
	Thu 27^{th} Feb	**Lab 1**	CAE-2
Week 2	Mon 03^{th} Mar	Lecture 1	
	Thu 06^{th} Mar	Lecture 2	
Week 3	Mon 10^{th} Mar	Lecture 3	
	Thu 13^{th} Mar	**Lab 2**	CAE-2
Week 4	Mon 17^{th} Mar	Lecture 4 (RJB)	
	Thu 20^{th} Mar	Lecture 5 (RJB)	
Week 5	Mon 24^{th} Mar	Lecture 6	

1^{st} Lab Thursday 27^{th} February 4.10 pm CAE-2

- L-Edit / T-Spice
  Hierarchical design, two conductor routing, simulation.
- Lab Book
  To be used for labs and throughout assignment.
  Also glue & scissors.
- Coloured Pencils

Red	Polysilicon
Green	N diffusion
Yellow / Brown	P diffusion
Blue	M1
Purple (Magenta)	M2
L.Blue (Cyan)	M3
Black	Contacts & Taps

  To be used in labs, assignment, lectures and **exam**.
- Arrange Assignment Teams

Assignment

Design and Implementation of a 4-bit Multiplier

- Stage 1 - Architecture and gate-level design
- Stage 2 - Leaf Cell Design and Characterization
- Stage 3 - Hierarchical layout

Assignment Schedule

Week 1	Mon 24^{th} Feb	**Assignment handed out**
Week 3	Fri 14^{th} Mar	**Checkpoint 1 report due** Architecture and gate-level schematics
Week 5	Fri 28^{th} Feb	**Checkpoint 2 report due** Leaf Cell Datasheets
Week 9	Mon 12^{th} May	**Final design due**
Week 10	Mon 19^{th} May	**Design report due**
Next Spring		Chips back from manufacture in USA