DESIGN SPECIFICATION

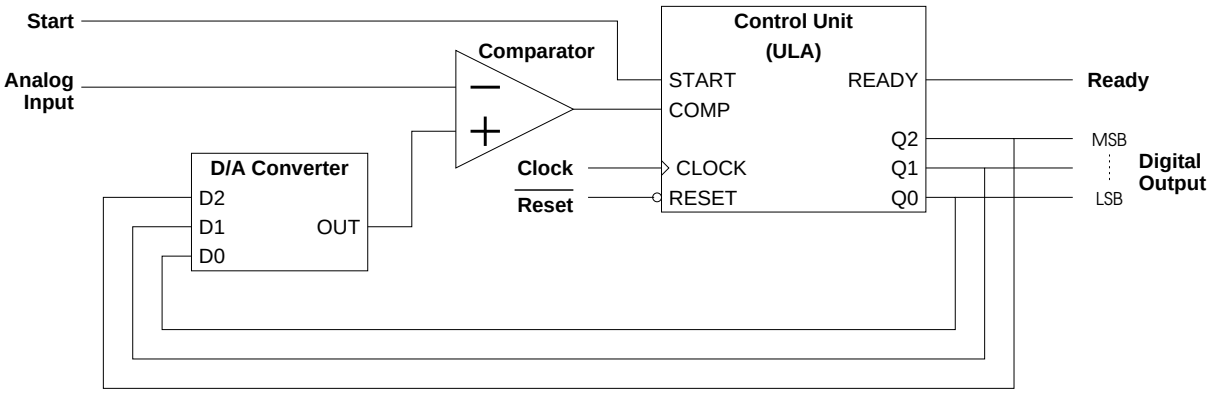
Introduction

This year's exercise is to design the control unit for a 3-bit successive approximation Analog to Digital Converter.

3-Bit Successive Approximation ADC

Successive approximation converters occupy the market between (slow and cheap) single slope converters and (fast and expensive) flash converters. They range normally between $100\mu s$ - $1\mu s$ conversion time and up to 14 bits in precision. The speed is achieved by successively setting and resetting bits of diminishing significance till the result is achieved.

A block diagram for the 3-bit ADC is shown below.

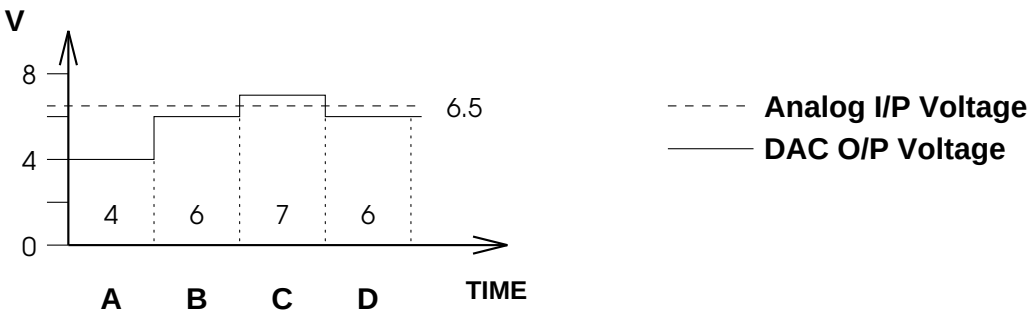


The control unit must find the largest number which is still less than the voltage at the analog input, based only on the information it receives from the comparator. In order to see how the converter works we will examine the behaviour of the converter as it attempts to convert an analog signal of 6.5v to its digital equivalent.[1]

[1] Assume that the 3-bit DAC gives a maximum output of 7.0v.

DESIGN SPECIFICATION

Let us consider what happens when the analog input is 6.5v:



- Cycle A
  - Set Q2 (Most significant bit).
  - This corresponds to a guess that the analog input is 4.0v.
  - The comparator output is low indicating that the analog input is greater than 4.0v.
  - In the next cycle we must increase our guess.
- Cycle B
  - Keep value of Q2. $\Rightarrow$ Q2 is now correct.
  - Set Q1.
  - This corresponds to a guess that the analog input is 6.0v.
  - The comparator output is low indicating that the analog input is greater than 6.0v.
  - In the next cycle we must increase our guess.
- Cycle C
  - Keep value of Q1. $\Rightarrow$ Q1 is now correct.
  - Set Q0.
  - This corresponds to a guess that the analog input is 7.0v.
  - The comparator output is high indicating that the analog input is less than 7.0v.
  - In the next cycle we must decrease our guess.
- Cycle D
  - Reset Q0 to 0. $\Rightarrow$ Q0 is now correct.
  - There are no more bits to set we have reached the correct answer.
  - Q2..Q0 shows 110 (6) indicating that the analog input is between 6.0v and 7.0v.

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Various solutions to this problem have been suggested in the past, not all of them are suitable for this design exercise. Your design for the control unit must satisfy the following specification:

- You can only use the gates which are available on the ULA:
  - AND_2 OR_2 XOR_2 XNOR_2 INV NAND_4 NAND_3 NAND_2 NOR_3 NOR_2
  - D_TYPE macro
- Synchronous Design:

  All designs must be fully synchronous. Major penalties will be incurred by teams who adopt asynchronous or quasi-synchronous design styles; as well as losing marks you will probably find that your design doesn't work.

  A fully synchronous design contains no spurious state elements; no RS flip-flops, no transparent latches and no feedback paths within combinational logic blocks. The only state elements will be the the edge triggered D-types as supplied in the ULA library.

- The design must support the following inputs and outputs
  - Inputs
    - CLOCK
      A single clock signal with an active rising edge is common to all D-types. You should not attempt to connect this signal to any gate input or output which is not labelled CLOCK.
    - nRESET
      A single active-low asynchronous reset signal is common to all D-types, this input is used for initialization only. You should not attempt to connect this signal to any gate input or output which is not labelled nRESET.
    - START
      CMOS compatible start conversion signal. This signal will go high for one clock cycle to indicate that the conversion should commence. The first comparison should be made during the next clock cycle after START goes high. START pulses will not be more frequent than one in every four clock cycles.
    - COMP
      CMOS compatible output from the comparator, high when the DAC output is greater than the Analog Input.

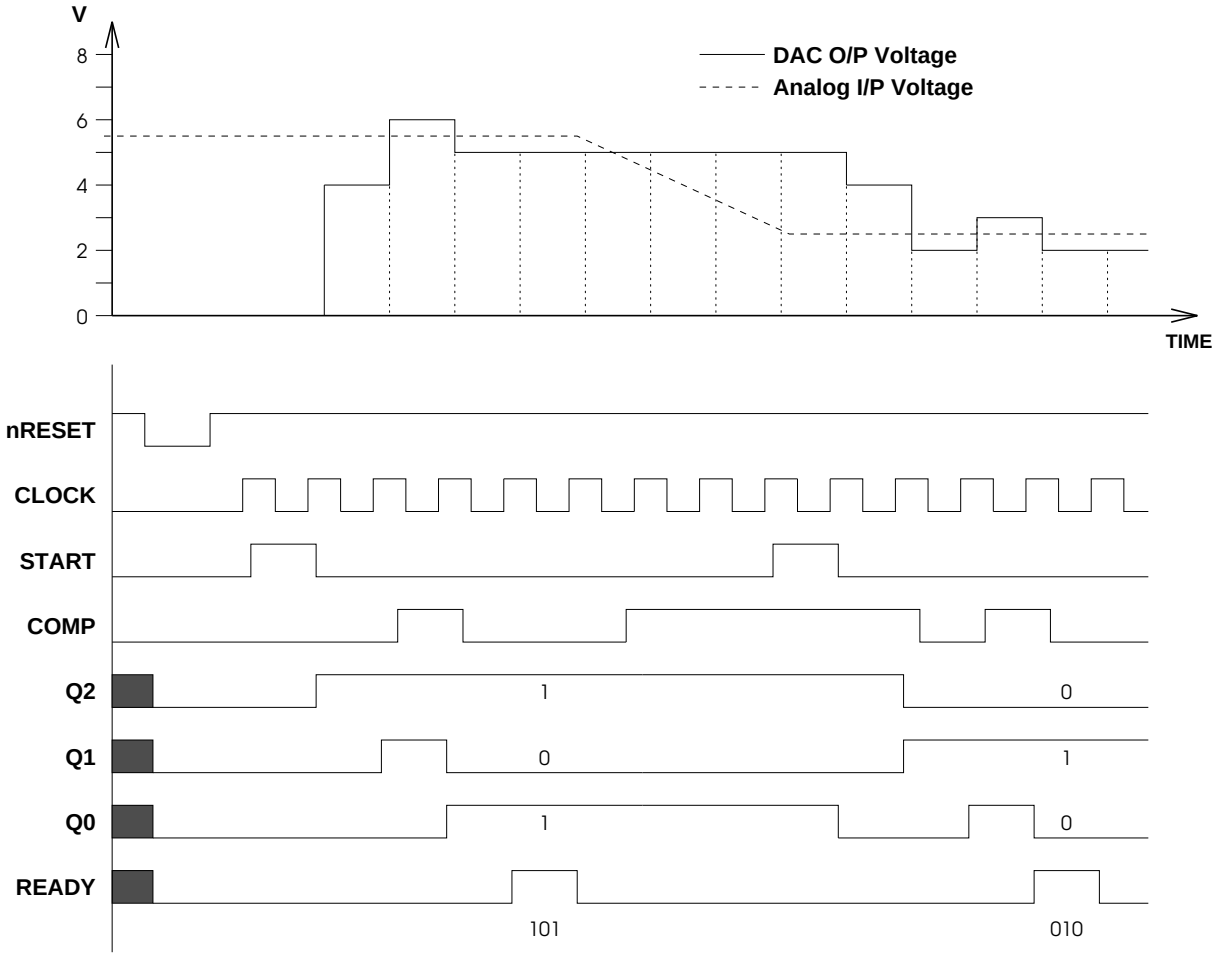
– Outputs

- - READY
  This signal must go high for one clock cycle to indicate that the conversion is complete. This cycle will coincide with the first cycle for which Q2..Q0 provide a valid result.

- - Q2..Q0
  These three outputs must drive the DAC during the conversion period and must give valid results between conversions. They should hold their value between the READY pulse indicating the end of one conversion and the START pulse indicating the beginning of the next.
  Q2 is the most significant bit.

Sample Waveform Diagram

In order to clarify the specification, the following diagram illustrates the behaviour of all of signals within the circuit, given a specific set of stimuli on the Analog Input, Clock and Reset lines:



In order for your circuit to meet the specification it is not necessary for it to follow exactly the timing diagram above, this diagram is for a specific implementation.
Nor is it sufficient that your circuit can exactly match the timing diagram, your design must function correctly for all sets of input stimuli.